WHAT IS CLAIMED IS:

1. A RAKE reception apparatus having a delay lock loop circuit, termed "DLL circuit", herein, for performing control to keep synchronization for a plurality of finger circuits adapted for separately despreading and demodulating reception signals passed through respective paths of the multiple paths, said apparatus comprising:

means for selecting one of the finger circuits which is to be an object of synchronous tracking in said DLL circuit based on the information at the time of output synthesis in a RAKE combiner adapted for combining outputs of said plural circuits with output demodulated signals; and

means for aligning the phase of said DLL circuit with the phase of the selected one finger circuit.

2. The RAKE reception apparatus as defined in claim 1 wherein

at the time of maximum ratio combining in said RAKE combiner, the finger circuit on which the maximum weighting is placed is selected based on the weighting information afforded to an output of said finger circuit.

3. The RAKE reception apparatus as defined in claim 1

wherein said DLL circuit includes means for detecting the correlation between a reference signal leading and lagging an optimal phase each by a preset timing, and a reception signal, and for varying the oscillation frequency of clocks based on the difference information of outputs of the correlation values, said clocks being supplied to a pseudorandom noise PN sequence generator in said DLL circuit adapted

for generating said leading and lagging reference signals and to said plural finger circuits; and

wherein

a shift register value of the PN sequence generator of the selected one of the finger circuits is loaded in a shift register of the PN sequence generator in said DLL circuit to align a code phase of said DLL circuit with a code phase of the selected one finger circuit.

4. The RAKE reception apparatus as defined in claim 2

wherein said DLL circuit includes means for detecting the correlation between a reference signal leading and lagging an optimal phase each by a preset timing, and a reception signal, and for varying the oscillation frequency of clocks based on the difference information of outputs of the correlation values, said clocks being supplied to a pseudorandom noise PN sequence generator in said DLL circuit adapted for generating said leading and lagging reference signals and to said plural finger circuits; and

wherein

a shift register value of the PN sequence generator of the selected one of the finger circuits is loaded in a shift register of the PN sequence generator in said DLL circuit to align a code phase of said DLL circuit with a code phase of the selected one finger circuit.

5. The RAKE reception apparatus as defined in claim 1

wherein said DLL circuit includes means for detecting the correlation between reference signals leading and lagging an optimal phase each by a preset timing, and a reception signal, and

means for varying the oscillation frequency of clocks based on the difference information of outputs of the correlation values;

said clocks being supplied to said plural finger circuits, and said DLL circuit being not provided with PN sequence generators;

said DLL circuit being fed with a reference signal leading and lagging a preset timing with respect to an optimal phase, said reference signal being output by the PN sequence generator of the selected one of the finger circuits, said DLL circuit using these reference signals for detecting the correlation with respect to the reception signal to align the code phase of said DLL circuit with the code phase of the selected one of the finger circuits.

6. The RAKE reception apparatus as defined in claim 2

wherein said DLL circuit includes means for detecting the correlation between reference signals leading and lagging an optimal phase each by a preset timing, and a reception signal, and

means for varying the oscillation frequency of clocks based on the difference information of outputs of the correlation values;

said clocks being supplied to said plural finger circuits, and said DLL circuit being not provided with PN sequence generators;

said DLL circuit being fed with a reference signal leading and lagging a preset timing with respect to an optimal phase, said reference signal being output by the PN sequence generator of the selected one of the finger circuits, said DLL circuit using these reference signals for detecting the correlation with respect to the reception signal to align the code phase of said DLL circuit with the code phase of the selected one of

the finger circuits.

7. A RAKE reception apparatus including:

a plurality of finger circuits for receiving signals spectrum-spread by spread codes and for despreading and demodulating respective reception signals retrieved by a searcher adapted for retrieving respective paths from multipath reception signals, and a RAKE combiner for combining demodulated outputs from said plural finger circuits,

said plural finger circuits not including a delay lock loop circuit , termed "DLL circuit", for synchronization holding controlling in its inside, but including a sole DLL circuit in common for said plural finger circuits; said RAKE reception apparatus comprising:

a changeover circuit for switching to one of said plural finger circuits to be synchronization tracked by said DLL circuit, among the plural finger circuits; and

a control circuit for receiving the finger-circuit-based information used by said RAKE combiner in combining outputs of said finger circuits, selecting said one of the finger circuits to be tracked by said DLL circuit, based on said information, and for commanding the switching to said changeover circuit.

8. The RAKE reception apparatus as defined in claim 7 wherein said control circuit selects the finger circuit, for which the maximum weighting is put, based on the finger-circuit-based weighting information output by said RAKE combiner, said control circuit commanding said changeover circuit to effect the switching to cause the DLL circuit to track the optimal finger circuit.

9. The RAKE reception apparatus as defined in claim 8 wherein said RAKE combiner combines the demodulated signals output by each finger circuit by a maximal ratio combining method.

10. The RAKE reception apparatus as defined in claim 7 wherein clocks output from said DLL circuit are routed not only to the one of the plural finger circuits selected by said changeover circuit but also to the remaining finger circuits.

11. The RAKE reception apparatus as defined in claim 10 wherein said clocks output from said DLL circuit are routed to the PN sequence generator of each finger circuit to perform synchronization holding operation.

12. The RAKE reception apparatus as defined in claim 7 wherein said DLL circuit receives an output signal of the one finger circuit selected by said changeover circuit and, based on the received signal, aligns the phase of the pseudorandom noise, termed "PN", code used for despreading the received data with the phase of the PN sequence generator in said one finger circuit selected by said changeover circuit.

13. The RAKE reception apparatus as defined in claim 7 wherein said DLL circuit receives an output signal of the one finger circuit selected by said changeover circuit and, based on the received signal, aligns the phase of the pseudorandom noise, termed "PN", code used for despreading the received data with the phase of the PN sequence generator in said one finger circuit selected by said changeover circuit,

wherein said control circuit selects the finger circuit, for which the maximum weighting is put, based on the finger-circuit-based weighting

information output by said RAKE combiner, said control circuit commanding said changeover circuit to effect the switching to cause the DLL circuit to track the optimal finger circuit,

wherein said RAKE combiner combines the demodulated signals output by each finger circuit by a maximal ratio combining method,

wherein clocks output from said DLL circuit are routed not only to the one of the plural finger circuits selected by said changeover circuit but also to the remaining finger circuits,

wherein said clocks output from said DLL circuit are routed to the PN sequence generator of each finger circuit to perform synchronization holding operation.

14. The RAKE reception apparatus as defined in claim 7 wherein the phase of the PN sequence generator in said DLL circuit is aligned to the phase of the PN sequence generator in the one finger circuit selected by said changeover circuit.

15. The RAKE reception apparatus as defined in claim 7 wherein the value of the shift register constituting the PN sequence generator of the selected one of the plural finger circuits is routed through said changeover circuit to said DLL circuit and wherein

the value of the shift register constituting the PN sequence generator in said DLL circuit is set to a value of the shift register input through said changeover circuit to align the phase of the PN sequence generator in said DLL circuit with the phase of the PN sequence generator in the selected one of the finger circuits.

16. The RAKE reception apparatus as defined in claim 7 wherein the PN

code string output by the PN sequence generator of the selected one of the plural finger circuits is routed through said changeover circuit to said DLL circuit and wherein

said DLL circuit despreads the reception data using the PN code string output from the PN sequence generator of the selected one finger circuit for phase alignment with respect to the PN sequence generator in the selected one finger circuit.

17. The RAKE reception apparatus as defined in claim 7 wherein said DLL circuit includes a PN sequence generator for generating and outputting an early PN code leading the PN code used in said finger circuit in timing and for generating and outputting a late PN code lagging the PN code used in said finger circuit in timing;

first and second multipliers for multiplying reception data with said early PN code and the late PN code, respectively;

first and second filters fed with outputs of said first and second multipliers, respectively;

first and second detectors for detecting outputs of said first and second filters, respectively;

a subtractor for subtracting an output of said second detector from an output of said first detector;

a loop filter for smoothing an output of said subtractor; and

a voltage-controlled oscillator fed with an output of said loop filter as a control voltage;

a shift register of said PN sequence generator of being loaded with a value of a shift register of the PN sequence generator of the one selected

finger circuit through said changeover circuit;

an output clock of said voltage-controlled oscillator being supplied to said PN sequence generator in said DLL circuit while being fed as a control clock to each of said finger circuits.

18. The RAKE reception apparatus as defined in claim 7 wherein

said finger circuit includes a PN sequence generator having the initial phase set from said searcher and generating the PN code;

a multiplier for multiplying input reception data with the PN sequence from said PN sequence generator; and

a low-pass filter for smoothing an output of said multiplier to output a demodulated signal; wherein

a value of the shift register constituting the PN sequence generator of the selected finger circuit is supplied through said changeover circuit to said DLL circuit.

19. The RAKE reception apparatus as defined in claim 12 wherein

said finger circuit includes a PN sequence generator having the initial phase set from said searcher and generating the PN code;

a multiplier for multiplying input reception data with the PN sequence from said PN sequence generator; and

a low-pass filter for smoothing an output of said multiplier to output a demodulated signal; wherein

a value of the shift register constituting the PN sequence generator of the selected finger circuit is supplied through said changeover circuit to said DLL circuit.

20. The RAKE reception apparatus as defined in claim 17 wherein

said finger circuit includes a PN sequence generator having the initial phase set from said searcher and generating the PN code;

a multiplier for multiplying input reception data with the PN sequence from said PN sequence generator; and

a low-pass filter for smoothing an output of said multiplier to output a demodulated signal; wherein

a value of the shift register constituting the PN sequence generator of the selected finger circuit is supplied through said changeover circuit to said DLL circuit.

21. The RAKE reception apparatus as defined in claim 7 in which said DLL circuit includes first and second multipliers for being fed with an early PN code and a late PN code output from the one finger circuit selected by said changeover circuit and for multiplying the reception data with said early PN code and said late PN code;

first and second filters for being fed with outputs of said first and second multipliers, respectively;

first and second detectors for detecting outputs of said first and second filters, respectively;

a subtractor for subtracting an output of said second detector from an output of said first detector;

a loop filter for smoothing an output of said subtractor; and

a voltage-controlled oscillator for being fed with an output of said loop filter as a control voltage; wherein

output clocks of said voltage-controlled oscillator is fed to said respective finger circuits.

22. The RAKE reception apparatus as defined in claim 7 wherein

said finger circuit includes a PN sequence generator having the initial phase set from said searcher and generating the PN code;

a multiplier for multiplying input reception data with the PN sequence from said PN sequence generator; and

a low-pass filter for smoothing an output of said multiplier to output a demodulated signal; wherein

said PN sequence generator is configured for generating an early PN code preceding the PN code in timing and a late PN code later in timing than the PN code used in said finger circuit, and for outputting the early and late PN codes to said changeover circuit.

23. The RAKE reception apparatus as defined in claim 21 wherein

said finger circuit includes a PN sequence generator having the initial phase set from said searcher and generating the PN code;

a multiplier for multiplying input reception data with the PN sequence from said PN sequence generator; and

a low-pass filter for smoothing an output of said multiplier to output a demodulated signal; wherein

said PN sequence generator is configured for generating an early PN code preceding the PN code in timing and a late PN code later in timing than the PN code used in said finger circuit, and for outputting the early and late PN codes to said changeover circuit.

24. The RAKE reception apparatus as defined in claim 7 wherein

said finger circuit includes a PN sequence generator having the initial phase set from said searcher and generating PN codes having an in-

phase component PNI and a quadrature component PNQ;

a complex multiplier for multiplying received input in-phase(I)/quadrature (Q) data with the PN sequence (PNI, PNQ) from said PN sequence generator; and

a low-pass filter for smoothing an output of said complex multiplier for outputting a demodulated signal.

25. The RAKE reception apparatus as defined in claim 7 wherein

said DLL circuit includes a PN sequence generator for generating and outputting early PN codes (an in-phase component PNI and a quadrature component PNQ) earlier in timing than the PN codes used in said finger circuit (an in-phase component PNI and a quadrature component PNQ) and for generating and outputting late PN codes (an in-phase component PNLI and a quadrature component PNLQ) later in timing than the PN codes used in said finger circuit (an in-phase component PNI and a quadrature component PNQ);

a first complex multiplier for multiplying received in-phase (I) and quadrature (Q) data with the PN codes (PNEI, PNEQ) generated by said PN sequence generator;

a second complex multiplier for multiplying received in-phase (I) and quadrature (Q) data with the PN codes (PNLI, PNLQ) generated by said PN sequence generator;

a first low-pass filter for smoothing an output of said first complex multiplier;

a second low-pass filter for smoothing an output of said second complex multiplier;

a first amplitude detector for detecting an output amplitude of said first low-pass filter;

a second amplitude detector for detecting an output amplitude of said second low-pass filter;

a subtractor for subtracting an output of said second amplitude detector from an output of said first amplitude detector;

a loop filter for smoothing an output of said subtractor; and

a voltage-controlled oscillator fed with an output of said subtractor as a control voltage; wherein

a value of a shift register of a PN sequence generator of said one finger circuit selected through said changeover circuit is loaded in the shift register of said PN sequence generator; and wherein

output clocks of said voltage-controlled oscillator are routed to said PN sequence generator and to said respective finger circuits.

26. The RAKE reception apparatus as defined in claim 7 wherein

said DLL circuit is fed via said changeover circuit with early PN codes (PNEI, PNEQ) and late PN codes (PNLI, PNLQ) output from the PN sequence generator of the selected one finger circuit; and includes:

a first complex multiplier for multiplying received in-phase (I)/quadrature (Q) data with said early PN codes (PNEI, PNEQ);

a second complex multiplier for multiplying received in-phase (I)/quadrature (Q) data with said late PN codes (PNLI, PNLQ);

a first low-pass filter for smoothing an output of said first complex multiplier;

a second low-pass filter for smoothing an output of said first

complex multiplier;

a first amplitude detector for detecting an output amplitude of said first low-pass filter;

a second amplitude detector for detecting an output amplitude of said second low-pass filter;

a subtractor for subtracting an output of said second amplitude detector from an output of said first amplitude detector;

a loop filter for smoothing an output of said subtractor; and

a voltage-controlled oscillator fed with an output of said loop filter as a control voltage; wherein

output clocks of said voltage-controlled oscillator is routed to said respective finger circuits.

27. The RAKE reception apparatus as defined in claim 7 wherein

said DLL circuit is fed via said changeover circuit with early PN codes (PNEI, PNEQ) and late PN codes (PNLI, PNLQ) output from the PN sequence generator of the selected one finger circuit; and includes:

a first complex multiplier for multiplying received in-phase (I)/quadrature (Q) data with said early PN codes (PNEI, PNEQ);

a second complex multiplier for multiplying received in-phase (I)/quadrature (Q) data with said late PN codes (PNLI, PNLQ);

a first low-pass filter for smoothing an output of said first complex multiplier;

a second low-pass filter for smoothing an output of said first complex multiplier;

a first amplitude detector for detecting an output amplitude of said

first low-pass filter;

a second amplitude detector for detecting an output amplitude of said second low-pass filter;

a subtractor for subtracting an output of said second amplitude detector from an output of said first amplitude detector;

a loop filter for smoothing an output of said subtractor; and

a voltage-controlled oscillator fed with an output of said loop filter as a control voltage; wherein

output clocks of said voltage-controlled oscillator is routed to said respective finger circuits,

wherein said control circuit selects the finger circuit, for which the maximum weighting is put, based on the finger-circuit-based weighting information output by said RAKE combiner, said control circuit commanding said changeover circuit to effect the switching to cause the DLL circuit to track the optimal finger circuit,

wherein said RAKE combiner combines the demodulated signals output by each finger circuit by a maximal ratio combining method,

wherein clocks output from said DLL circuit are routed not only to the one of the plural finger circuits selected by said changeover circuit but also to the remaining finger circuits,

wherein said clocks output from said DLL circuit are routed to the PN sequence generator of each finger circuit to perform synchronization holding operation,

wherein said DLL circuit receives an output signal of the one finger circuit selected by said changeover circuit and, based on the received

signal, aligns the phase of the pseudorandom noise, termed "PN", code used for despreading the received data with the phase of the PN sequence generator in said one finger circuit selected by said changeover circuit.

28. The RAKE reception apparatus as defined in claim 1 wherein one or a plurality of said DLL circuits are provided each one of which is provided in each group of a plurality of finger circuits.

29. The RAKE reception apparatus as defined in claim 7 wherein one or a plurality of said DLL circuits are provided each one of which is provided in each group of a plurality of finger circuits.